CLAIMS:

I claim:

1. A memory device die or chip testing, sorting, and packaging system comprising:

(a) a plurality of test processing units;

(b) a plurality of test connection units;

(c) a plurality of test messaging units;

(d) a plurality of sorting control units;

(e) a plurality of sorting output units;

(f) a plurality of packaging units;

(g) a plurality of packaging control units;

wherein said test processing unit performs tests on at least one memory device placed on at least one said test connection unit and identifies the memory device type or configuration according to the test results;

wherein said memory device type or configuration information is forwarded from said processing unit to at least one said test messaging unit, said device information may subsequently be forwarded directly or indirectly to at least one said sorting control unit or at least one said packaging control unit;

wherein said memory device is transferred to one said sorting output unit according to the instruction from one said sorting control unit based on the memory device information directly or indirectly from said test messaging unit;

wherein one or more of said memory devices are packaged into memory chips or memory modules in one said packaging unit according to the instruction from one said packaging control unit based on the memory device information directly or indirectly from said test messaging unit or said sorting control unit.

2. The memory device or chip testing, sorting, and packaging system of claim 1, wherein said test processing unit is an in-circuit memory system, a special memory tester, or an automatic test equipment.

3. The memory device or chip testing, sorting, and packaging system of claim 1, wherein said test connection unit is a die probing card, a chip socket, a connector, an adaptor, or a printed circuit board with passive, active, or logic components.

4. The memory device or chip testing, sorting, and packaging system of claim 1, wherein said test messaging unit is a printing device, a memory device, a storage device, or an electrical, optical, or wireless communication link.

5. The memory device or chip testing, sorting, and packaging system of claim 1, wherein said sorting output unit is a plurality of output trays, each contains a plurality of output entry cells.

6. The memory device or chip testing, sorting, and packaging system of claim 1, wherein said sorting control unit contains a plurality of position selection indicators, each located next to an output tray or an output entry cell, said sorting control unit accepts device information and lights up a position selection indicator

to identify a selected output tray or a selected output entry cell to place the memory device.

7. The memory device or chip testing, sorting, and packaging system of claim 1, wherein said sorting control unit accepts device information and controls an automatic routing unit to transfer said memory device to the selected output tray or output entry cell.

8. The memory device or chip testing, sorting, and packaging system of claim 1, wherein said sorting control unit contains a plurality of position sensors, each located next to a output tray or a output entry cell, said sorting control unit monitors the status of the output trays or output entry cells to determine whether a memory device is properly placed in the selected position.

9. The memory device or chip testing, sorting, and packaging system of claim 1, wherein said sorting control unit maintains a memory device configuration mapping information and determines whether some matching groups of the memory devices are to be placed in selected sorted configuration output trays or output entry cells.

10. The memory device or chip testing, sorting, and packaging system of claim 1, wherein said packaging unit is a wire bonding machine, a multiple-chip module assembly machine, or a printed circuit board assembly machine.

11. The memory device or chip testing, sorting, and packaging system of claim 1, wherein said packaging control unit accepts device information and

controls the packaging unit to perform the wire bonding, component placement, or circuit assembly according to the device type and configuration.

12. The memory device or chip testing, sorting, and packaging system of claim 1, further comprises a plurality of detachable memory device carrier units to transport memory devices between a test connection unit, a sorting output unit, or a packaging unit, said device carrier unit contains a plurality of device carrier entry cells, a plurality of device descriptions in the form of printed label or memory storage, and an interface unit to send or receive device description to or from a test messaging unit, a sorting control unit, or a packaging control unit.

13. The memory device or chip testing, sorting, and packaging system of claim 1, wherein said output tray is detachable from the sorting unit.

14. The memory device or chip testing, sorting, and packaging system of claim 1, wherein said output tray contains a plurality of device entry cells, a plurality of device descriptions in the form of printed label or memory storage, and an interface unit to send or receive device description.

15. The memory device or chip testing, sorting, and packaging system of claim 1, wherein said tested memory devices are first being sorted and then being packaged.

16. The memory device or chip testing, sorting, and packaging system of claim 1, wherein said tested memory devices are first being packaged and then being sorted.

17. A memory device die or chip testing and sorting system comprising:

(a) a plurality of test processing units;

(b) a plurality of test connection units;

(c) a plurality of test messaging units;

(d) a plurality of sorting control units;

(e) a plurality of sorting output units;

wherein said test processing unit performs tests on at least one memory device placed on at least one said test connection unit and identifies the memory device type or configuration according to the test results;

wherein said memory device type or configuration information is forwarded from said processing unit to at least one said test messaging unit, said device information may subsequently be forwarded directly or indirectly to at least one said sorting control unit;

wherein said memory device is transferred to one said sorting output unit according to the instruction from one said sorting control unit based on the memory device information directly or indirectly from said test messaging unit.

18. The memory device or chip testing and sorting system of claim 17, wherein said test processing unit is an in-circuit memory system, a special memory tester, or an automatic test equipment.

19. The memory device or chip testing and sorting system of claim 17, wherein said test connection unit is a die probing card, a chip socket, a connector, an adaptor, or a printed circuit board with passive, active, or logic components.

20. The memory device or chip testing and sorting system of claim 17, wherein said test messaging unit is a printing device, a memory device, a storage device, or an electrical, optical, or wireless communication link.

21. The memory device or chip testing and sorting system of claim 17, wherein said sorting output unit is a plurality of output trays, each contains a plurality of output entry cells.

22. The memory device or chip testing and sorting system of claim 17, wherein said sorting control unit contains a plurality of position selection indicators, each located next to an output tray or an output entry cell, said sorting control unit accepts device information and lights up a position selection indicator to identify a selected output tray or a selected output entry cell to place the memory device.

23. The memory device or chip testing and sorting system of claim 17, wherein said sorting control unit accepts device information and controls an automatic routing unit to transfer said memory device to the selected output tray or output entry cell.

24. The memory device or chip testing and sorting system of claim 17, wherein said sorting control unit contains a plurality of position sensors, each located next to a output tray or a output entry cell, said sorting control unit monitors the status of the output trays or output entry cells to determine whether a memory device is properly placed in the selected position.

25. The memory device or chip testing and sorting system of claim 17, wherein said sorting control unit maintains a memory device configuration

mapping information and determines whether some matching groups of the memory devices are to be placed in selected sorted configuration output trays or output entry cells.

26. The memory device or chip testing and sorting system of claim 17, further comprises a plurality of detachable memory device carrier units to transport memory devices between a test connection unit and a sorting output unit, said device carrier unit contains a plurality of device carrier entry cells, a plurality of device descriptions in the form of printed label or memory storage, and an interface unit to send or receive device description to or from a test messaging unit or a sorting control unit.

27. The memory device or chip testing and sorting system of claim 17, wherein said output tray is detachable from the sorting unit.

28. The memory device or chip testing and sorting system of claim 17, wherein said output tray contains a plurality of device entry cells, a plurality of device descriptions in the form of printed label or memory storage, and an interface unit to send or receive device description.

29. A memory device die or chip sorting system comprising:

(a) a plurality of sorting output units;

(b) a plurality of sorting control units;

(c) a plurality of input interface units;

wherein said sorting output unit contains a plurality of output trays, each contains a plurality of output entry cells;

wherein said sorting control unit accepts memory device type or configuration information through said input interface;

wherein said memory device is transferred to one said sorting output unit according to the instruction from one said sorting control unit based on the memory device information.

30. The memory device or chip sorting system of claim 29, wherein said device information is in the form of printed label, memory storage, or electrical, optical, or wireless communication signals.

31. The memory device or chip sorting system of claim 29, wherein said sorting control unit contains a plurality of position selection indicators, each located next to an output tray or an output entry cell, said sorting control unit accepts device information and lights up a position selection indicator to identify a selected output tray or a selected output entry cell to place the memory device.

32. The memory device or chip sorting system of claim 29, wherein said sorting control unit accepts device information and control an automatic routing unit to transfer said memory device to the selected output tray or output entry cell.

33. The memory device or chip sorting system of claim 29, wherein said sorting control unit contains a plurality of position sensors, each located next to a output tray or a output entry cell, said sorting control unit monitors the status of the output trays or output entry cells to determine whether a memory device is properly placed in the selected position.

34. The memory device or chip sorting system of claim 29, wherein said sorting control unit maintains a memory device configuration mapping information and determines whether some matching groups of the memory devices are to be placed in selected sorted configuration output trays or output entry cells.

35. The memory device or chip sorting system of claim 29, further comprises a plurality of detachable memory device carrier unit to transport memory devices to said sorting output unit, said device carrier unit contains a plurality of device carrier entry cells, a plurality of device descriptions in the form of printed label or memory storage, and an interface unit to send or receive device description.

36. The memory device or chip sorting system of claim 29, wherein said output tray is detachable from the sorting unit.

37. The memory device or chip sorting system of claim 29, wherein said output tray contains a plurality of device entry cells, a plurality of device descriptions in the form of printed label or memory storage, and an interface unit to send or receive device description.